



# HEF4071B

Quad 2-input OR gate

Rev. 9.1 — 19 October 2023

Product data sheet

## 1. General description

The HEF4071B is a quad 2-input OR gate. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of  $V_{DD}$ .

## 2. Features and benefits

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- CMOS low power dissipation
- High noise immunity
- Standardized symmetrical output characteristics
- Inputs and outputs are protected against electrostatic effects
- Complies with JEDEC standard JESD 13-B
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-B exceeds 200 V
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$  and  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$

## 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
<a href="#">HEF4071BT</a>	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	SO14	plastic small outline package; 14 leads; body width 3.9 mm	<a href="#">SOT108-1</a>

## 4. Functional diagram

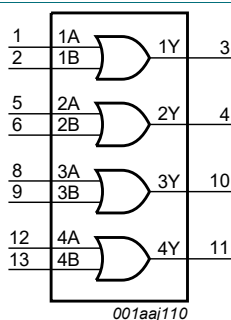


Fig. 1. Functional diagram

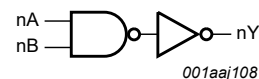
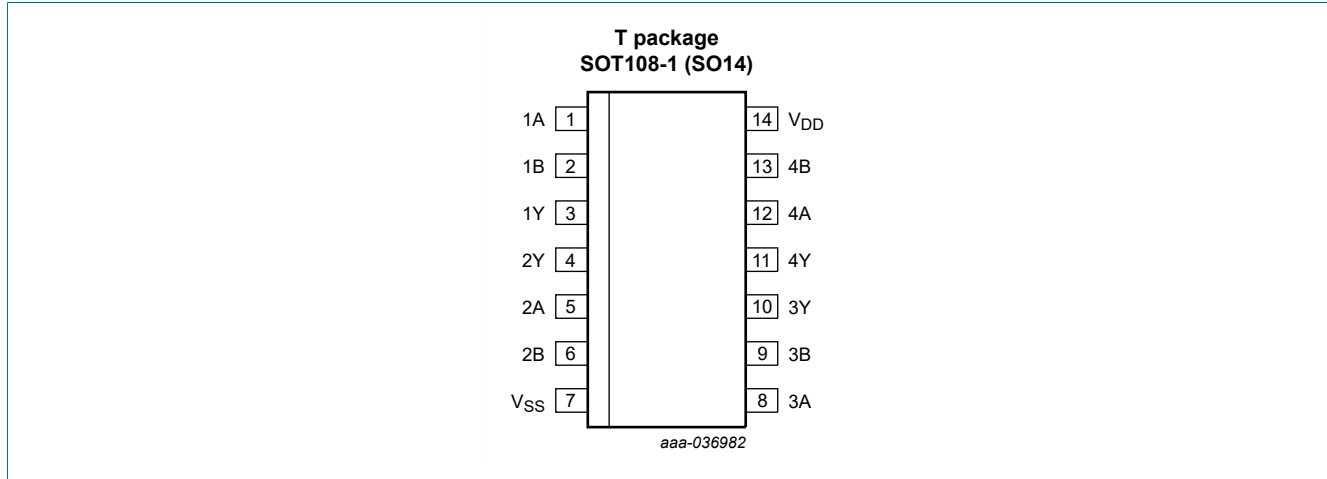


Fig. 2. Logic diagram (one gate)

## 5. Pinning information

### 5.1. Pinning



### 5.2. Pin description

**Table 2. Pin description**

Symbol	Pin	Description
1A , 2A, 3A, 4A	1, 5, 8, 12	input
1B, 2B, 3B, 4B	2, 6, 9, 13	input
1Y, 2Y, 3Y, 4Y	3, 4, 10, 11	output
V <sub>SS</sub>	7	ground (0 V)
V <sub>DD</sub>	14	supply voltage

## 6. Functional description

**Table 3. Function table**

*H = HIGH voltage level; L = LOW voltage level.*

Input		Output
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	H

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to  $V_{SS} = 0$  V (ground).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD}$	supply voltage		-0.5	+18	V
$I_{IK}$	input clamping current	$V_I < -0.5$ V or $V_I > V_{DD} + 0.5$ V	-	$\pm 10$	mA
$V_I$	input voltage		-0.5	$V_{DD} + 0.5$	V
$I_{OK}$	output clamping current	$V_O < -0.5$ V or $V_O > V_{DD} + 0.5$ V	-	$\pm 10$	mA
$I_{I/O}$	input/output current		-	$\pm 10$	mA
$I_{DD}$	supply current		-	50	mA
$T_{stg}$	storage temperature		-65	+150	°C
$T_{amb}$	ambient temperature		-40	+125	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to + 125 °C [1]	-	500	mW
$P$	power dissipation	per output	-	100	mW

[1] For SOT108-1 (SO14) package:  $P_{tot}$  derates linearly with 10.1 mW/K above 100 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD}$	supply voltage		3	15	V
$V_I$	input voltage		0	$V_{DD}$	V
$T_{amb}$	ambient temperature	in free air	-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{DD} = 5$ V	-	3.75	$\mu\text{s/V}$
		$V_{DD} = 10$ V	-	0.5	$\mu\text{s/V}$
		$V_{DD} = 15$ V	-	0.08	$\mu\text{s/V}$

## 9. Static characteristics

**Table 6. Static characteristics**

$V_{SS} = 0$  V;  $V_I = V_{SS}$  or  $V_{DD}$ , unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$	$T_{amb} = -40$ °C		$T_{amb} = +25$ °C		$T_{amb} = +85$ °C		$T_{amb} = +125$ °C		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	$ I_O  < 1$ $\mu\text{A}$	5 V	3.5	-	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	11.0	-	V
$V_{IL}$	LOW-level input voltage	$ I_O  < 1$ $\mu\text{A}$	5 V	-	1.5	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	-	4.0	V
$V_{OH}$	HIGH-level output voltage	$ I_O  < 1$ $\mu\text{A}$	5 V	4.95	-	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	14.95	-	V

Symbol	Parameter	Conditions	V <sub>DD</sub>	T <sub>amb</sub> = -40 °C		T <sub>amb</sub> = +25 °C		T <sub>amb</sub> = +85 °C		T <sub>amb</sub> = +125 °C		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
V <sub>OL</sub>	LOW-level output voltage	I <sub>O</sub>   < 1 μA	5 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	-	0.05	V
I <sub>OH</sub>	HIGH-level output current	V <sub>O</sub> = 2.5 V	5 V	-	-1.7	-	-1.4	-	-1.1	-	-1.1	mA
		V <sub>O</sub> = 4.6 V	5 V	-	-0.64	-	-0.5	-	-0.36	-	-0.36	mA
		V <sub>O</sub> = 9.5 V	10 V	-	-1.6	-	-1.3	-	-0.9	-	-0.9	mA
		V <sub>O</sub> = 13.5 V	15 V	-	-4.2	-	-3.4	-	-2.4	-	-2.4	mA
I <sub>OL</sub>	LOW-level output current	V <sub>O</sub> = 0.4 V	5 V	0.64	-	0.5	-	0.36	-	0.36	-	mA
		V <sub>O</sub> = 0.5 V	10 V	1.6	-	1.3	-	0.9	-	0.9	-	mA
		V <sub>O</sub> = 1.5 V	15 V	4.2	-	3.4	-	2.4	-	2.4	-	mA
I <sub>I</sub>	input leakage current		15 V	-	±0.1	-	±0.1	-	±1.0	-	±1.0	μA
I <sub>DD</sub>	supply current	all valid input combinations; I <sub>O</sub> = 0 A	5 V	-	0.25	-	0.25	-	7.5	-	7.5	μA
			10 V	-	0.5	-	0.5	-	15.0	-	15.0	μA
			15 V	-	1.0	-	1.0	-	30.0	-	30.0	μA
C <sub>I</sub>	input capacitance			-	-	-	7.5	-	-	-	pF	

## 10. Dynamic characteristics

Table 7. Dynamic characteristics

T<sub>amb</sub> = 25 °C, unless otherwise specified. For waveforms see Fig. 3; for test circuit see Fig. 4.

Symbol	Parameter	Conditions	V <sub>DD</sub>	Extrapolation formula [1]	Min	Typ	Max	Unit
t <sub>PHL</sub>	HIGH to LOW propagation delay	nA or nB to nY	5 V	28 ns + (0.55 ns/pF)C <sub>L</sub>	-	55	115	ns
			10 V	15 ns + (0.23 ns/pF)C <sub>L</sub>	-	25	50	ns
			15 V	12 ns + (0.16 ns/pF)C <sub>L</sub>	-	20	35	ns
t <sub>PLH</sub>	LOW to HIGH propagation delay	nA or nB to nY	5 V	18 ns + (0.55 ns/pF)C <sub>L</sub>	-	45	90	ns
			10 V	9 ns + (0.23 ns/pF)C <sub>L</sub>	-	20	45	ns
			15 V	7 ns + (0.16 ns/pF)C <sub>L</sub>	-	15	30	ns
t <sub>t</sub>	transition time		5 V	[2] 10 ns + (1.00 ns/pF)C <sub>L</sub>	-	60	120	ns
			10 V	[2] 9 ns + (0.42 ns/pF)C <sub>L</sub>	-	30	60	ns
			15 V	[2] 6 ns + (0.28 ns/pF)C <sub>L</sub>	-	20	40	ns

[1] The typical value of the propagation delay and output transition time can be calculated with the extrapolation formula (C<sub>L</sub> in pF).

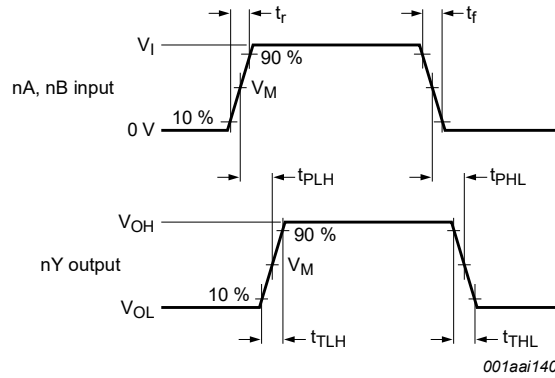
[2] t<sub>t</sub> is the same as t<sub>THL</sub> and t<sub>TLH</sub>.

Table 8. Dynamic power dissipation

V<sub>SS</sub> = 0 V; t<sub>r</sub> = t<sub>f</sub> ≤ 20 ns; T<sub>amb</sub> = 25 °C.

Symbol	Parameter	V <sub>DD</sub>	Typical formula	where:
P <sub>D</sub>	dynamic power dissipation	5 V	P <sub>D</sub> = 1150 × f <sub>i</sub> + Σ(f <sub>o</sub> × C <sub>L</sub> ) × V <sub>DD</sub> <sup>2</sup> (μW)	f <sub>i</sub> = input frequency in MHz; f <sub>o</sub> = output frequency in MHz; C <sub>L</sub> = output load capacitance in pF; Σ(f <sub>o</sub> × C <sub>L</sub> ) = sum of the outputs; V <sub>DD</sub> = supply voltage in V.
		10 V	P <sub>D</sub> = 4800 × f <sub>i</sub> + Σ(f <sub>o</sub> × C <sub>L</sub> ) × V <sub>DD</sub> <sup>2</sup> (μW)	
		15 V	P <sub>D</sub> = 19700 × f <sub>i</sub> + Σ(f <sub>o</sub> × C <sub>L</sub> ) × V <sub>DD</sub> <sup>2</sup> (μW)	

10.1. Waveforms and test circuit

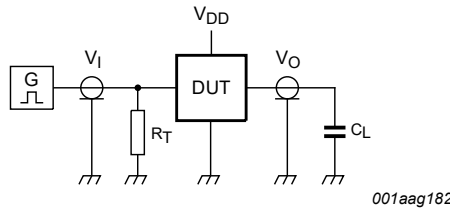


Measurement points are given in [Table 9](#).  
 Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

Fig. 3. Input to output propagation delay and output transition times

Table 9. Measurement points

Supply voltage	Input	Output
$V_{DD}$	$V_M$	$V_M$
5 V to 15 V	$0.5 \times V_{DD}$	$0.5 \times V_{DD}$



Test data is given in [Table 10](#).  
 Definitions for test circuit:  
 $C_L$  = load capacitance including jig and probe capacitance;  
 $R_T$  = termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator.

Fig. 4. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input	Load
$V_{DD}$	$V_I$	$C_L$
5 V to 15 V	$V_{SS}$ or $V_{DD}$	$\leq 20$ ns
		50 pF

### 11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

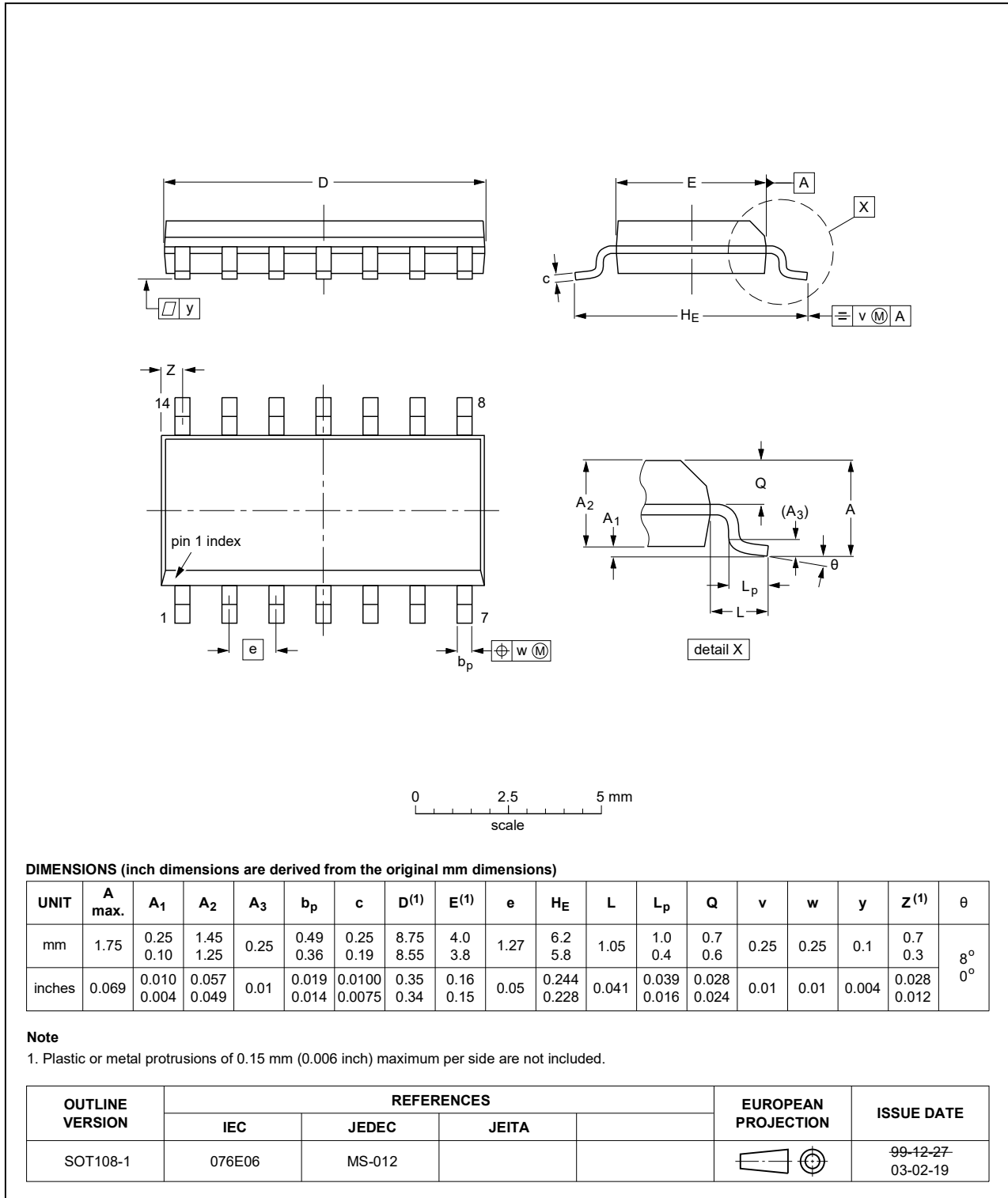


Fig. 5. Package outline SOT108-1 (SO14)

## 12. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

## 13. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4071B v.9.1	20231019	Product data sheet	-	HEF4071B v.8
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Table 4</a>: Derating values for <math>P_{tot}</math> total power dissipation updated.</li> <li><a href="#">Section 1</a> and <a href="#">Section 2</a> updated.</li> </ul>			
HEF4071B v.8	20151216	Product data sheet	-	HEF4071B v.7
Modifications:	<ul style="list-style-type: none"> <li>Type number HEF4071BP (SOT27-1) removed.</li> </ul>			
HEF4071B v.7	20111115	Product data sheet	-	HEF4071B v.6
Modifications:	<ul style="list-style-type: none"> <li>Section Applications removed.</li> <li><a href="#">Table 6</a>: <math>I_{OH}</math> minimum values changed to maximum.</li> </ul>			
HEF4071B v.6	20091201	Product data sheet	-	HEF4071B v.5
HEF4071B v.5	20090728	Product data sheet	-	HEF4071B v.4
HEF4071B v.4	20081128	Product data sheet	-	HEF4071B_CNV v.3
HEF4071B_CNV v.3	19950101	Product specification	-	HEF4071B_CNV v.2
HEF4071B_CNV v.2	19950101	Product specification	-	-

## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 19 October 2023

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